

ADC_3117

High-Density ADC FMC

Technical Specification

SUMMARY:

This document provides the technical specification of the , a High-Density ADC in FMC form factor featuring 20 ADC channels with 16-bit resolution at sampling rates of 2 / 5 Msps and 2 DAC outputs.

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ADC_3117 High-Density ADC FMC

Technical Specification

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0.1.0	23 Nov 2016	Technical specification updated with new pinout and electrical schematics	CG	IG	JB

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1. Introduction

1.1 Purpose

This document provides the technical specification of the , a High-Density ADC in FMC form factor featuring 20 ADC channels with 16-bit resolution at sampling rates of 2 / 5 Msps and 2 DAC outputs.

1.2 Scope

This Technical Specification provides the following:

- Product description
- Mechanical information
- FPGA firmware support

1.3 Acronyms and Abbreviations

Acronym	Definition
BOM	Bill Of Materials
CPU	Central Processing Unit
ESD	Electrostatic Discharge
FMC	FPGA Mezzanine Card
FPGA	Field Programmable Gate Array
GbE	Gigabit Ethernet
Gbps	Gigabits per second
GBps	Gigabytes per second
HPC	High-Pin Count
IFC	Intelligent FMC Carrier
IFC	Intelligent FPGA Controller
I/F	Interface
I/O	Input/Output
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LPC	Low Pin Count
MTCA or MicroTCA	A PICMG specification in which AMC Modules plug directly into a backplane.
MTBF	Mean Time Between Failure(s)
PCB	Printed Circuit Board
RoHS	Restriction of the Use of Certain Hazardous Substances

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Acronym	Definition
SBC	Single Board Computer
SFP	Small Form Factor Pluggable, a type of packaging for I/O physical layer components, typically optical I/O components
SerDes	Serializer-Deserializer

Table 1.1 - Acronyms

1.4 Technical References

Component	Description	Supplier
LTC2323-16 LTC2323-14	Dual channel 16-bit ADC up to 5 Msps Dual channel 14-bit ADC up to 5 Msps	LINEAR
ADG1204	4:1 Analog multiplexer Low Capacitance, Low Charge Injection, ± 15 V/ ± 12 V, 4:1 iCMOS Multiplexer	AD
AD5290	Compact +30V / ± 15 V 256-Position Digital Potentiometer	AD
AD8250	10 MHz, 20 V/ μ s, G = 1, 2, 5, 10 iCMOS Programmable Gain Instrumentation Amplifier	AD
AD8475	Precision, Selectable Gain, Fully Differential Funnel Amplifier	AD
ADA4075-2	Low noise amplifier	AD
LMV842	Dual CMOS Input, RRIO, Low Power, Wide Supply Range, 4.5-MHz Operational Amplifiers	TI
DAC8563T	Low-Noise Clock Jitter Cleaner with Dual Loop PLLs	TI
REF5010	Low Noise, Very Low Drift, Precision Voltage Reference	TI
LMK04803	Low-Noise Clock Jitter Cleaner with Dual Loop PLLs	TI
SY58611U	3.2Gbps Precision, LVDS 2:1 Mux with internal termination and Fail Safe Input	MICREL
TS3A44159	0.45 Ω Quad SPDT Analog Switch 4-Channel 2:1 Multiplexer-Demultiplexer with two controls	TI
SN65LVDS1	SN65LVDxx High-Speed Differential Line Drivers and Receivers	TI
SN65LVDT2	SN65LVDxx High-Speed Differential Line Drivers and Receivers	TI
TPS7A4700	36-V, 1-A, 4- μ V _{RMS} , RF LDO Voltage Regulator	TI
TPS55340RTE	Integrated 5-A Wide Input Range Boost/SEPIC/Flyback DC-DC Regulator	TI
TPS7A3301	-36 V, 1-A, Ultra low-Noise Negative Voltage Regulator	TI
TPS63700DRC	DC-DC Inverter	TI
XRA1405	SPI 25MHz GPIO expander	EXAR
CVHD-037-100MHz	CMOS Voltage Controlled Crystal Oscillator 100Mhz / 50 ppm	Crystak
TMP102	Low-Power Digital Temperature Sensor With SMBus and Two-Wire Serial Interface	TI
M24256	256-Kbit serial I ² C bus EEPROM	ST
3M SDR 26p connector	3M Shrunk Delta Ribbon Connector Part No. 12226-8250-00FR	3M

Table 1.2 - ADC_3117 Components Reference

1.5 IOxOS References

Following table summarizes the related IOxOS Products.

Related Products	Product Description
ADC_3110	Eight-channel 16-bit @ 250Msps AC-coupled analog to digital converter
ADC_3111	Eight-channel 16-bit @ 250Msps DC-coupled analog to digital converter
ADC_3112	Four-channel 12-bit @ 1000Msps DC-coupled analog to digital converter
DAC_3113	Dual-channel 16-bit @ 500Msps digital to analog converter
DAC_3114	Dual-channel 16-bit @ 500Msps digital to analog converter with ultra low jitter clock distribution
IFC_1210	IOxOS PowerPC P2020 VME64X Single Board Computer with dual FMC slots
IFC_1211	IOxOS PowerPC T2081 VME64X Single Board Computer with dual FMC slots
IFC_1410	IOxOS PowerPC T2081 MTCA.4 AMC with dual FMC slots
TOSCA III	FPGA Design Kit

Table 1.3 - IOxOS Related Products References

1.6 Specification Reference

Following table records the references to technical specifications mentioned in this document.

Reference	Reference	Comments	Source
[VITA57.1]	VITA 57.1-2008	FMC specifications	VITA

Table 1.4 - Specification References

2. ADC_3117 Product Overview

The following sections provide the technical description of the ADC_3117 High-Density ADC.

2.1 General Information

2.1.1 ADC_3117 Ordering Informations

Following ordering options are available:

Reference	Dimension	Environmental
	20 channels 16-bit ADC 10[mm] FMC stacking	Commercial (0-50 [°C])
	20 channels 16-bit ADC 8.5[mm] FMC stacking	Commercial (0-50 [°C])
ADC3117_FDK	ADC_3117 TOSCA Integration (VHDL source code)	

Table 2.1 - ADC_3117 Options & Ordering Informations

2.1.2 Power Requirements

The has the following power requirements when operating at commercial temperature grade (0 - 50 [°C]):

- Typical Power dissipation ~4 [W] (6 [W] Max.)
- FMC ANSI/VITA 57.1 Power requirements
 - 3P3V / 1.200 [A]
 - 3P3VAUX / 0.003 [A]
 - 12P0V / 0.145 [A]
 - VADJ / 0.003 [A]

2.1.3 Environmental

The is available in Commercial temperature grade (0-50 [°C]).

Industrial/extended temperature range available upon request.

2.2 Technical Description

The ADC_3117 is a single width FMC ANSI/VITA57.1 providing twenty(20) DC coupled ADC channels with 16-bit resolution at a sampling rate up to 5 Msps. The conversion signalling can be controlled from the FPGA user application or/and from the front panel connector signalling.

The digital back-end interface to the FPGA is implemented with differential LVDS providing optimal noise protection.

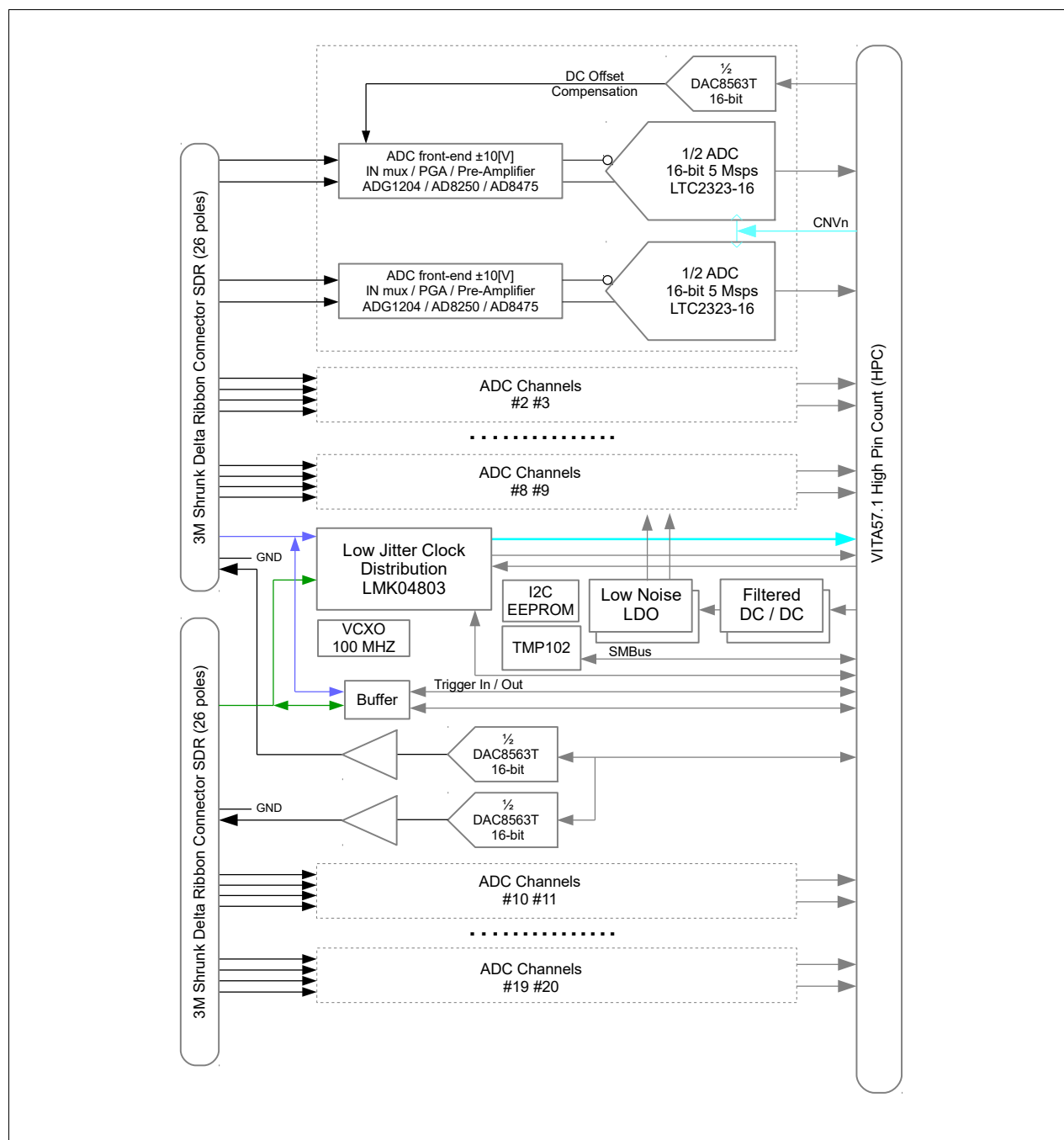


Figure 1 - ADC_3117 Block Diagram

Key features

- Single-width FMC ANSI/VITA57.1 HPC Mezzanine card
 - Optional equipment for 8.5[mm] HPC-8.5 stacking full-filling the MTCA.4 4U unit
- Twenty(20) channels ADC 16-bit / 14-bit up to 5 Msps
 - Latest generation Linear technology LTC2323-16/14
 - Optional lower cost LTC2321-16/14 (pin/package compatible with LTC2323)
 - Selectable Differential / Single-Ended mode
 - Selectable gain: $\pm 10V$, $\pm 5V$, $\pm 2V$, $\pm 1V$.
 - DAC for offset compensation ($\pm 10V$)
- Two(2) Analog Outputs driven from 16-bit DAC8563T
 - $\pm 0..10V$ output range
- On-board calibration reference voltage
- Maximum 6 [W] power dissipation
- Two(2) 3M Shrunk Delta Ribbon (SDR) Right Angle Connectors
 - 20x ADC inputs (differential or single-ended)
 - 2x DAC outputs
 - 2x Clock References / Triggers (Inputs / Outputs)
- Complete FPGA Design Kit for ADC read-out, clock distribution management
- Miscellaneous
 - I2C EEPROM connected on FMC SMBus
 - Temperature Monitoring TMP102 connected on FMC SMBus
 - Low noise LDO for on-board ADC power supplies
 - Fully differential FPGA back-end interface (LVDS)

2.2.1 ADC IO Connector

The ADC_3117 front panel is equipped with two SDR connectors from 3M, allowing to stack at 8.5[mm] as required for MTCA.4 implementation.

The two 26 poles 3M Shrunk Delta Ribbon connectors provide:

- 20 x ADC input channels (2 poles for each channels)
- 2 x DAC Outputs
- 2 x External Clock Reference / Trigger Input/Output

2.2.2 Data Acquisition ADC Chain

The ADC_3117 implements a specific front-end for each ADC channel

- A $\pm 100V$ input protection ($\pm 100V$ continuous, $\pm 500V$ peak),
- A differential input with $1\text{ M}\Omega$ (or higher) resistance to GND;
- A pair of input multiplexer to select between direct input, GND, offset or calibration voltage (VCAL);
- A high impedance instrumentation amplifier with programmable gain (1, 2, 5 or 10);
- A fully differential amplifier to process the signal for the high resolution ADC with differential drive with the correct common mode voltage;
- A low pass filter to limit the bandwidth just at the minimum needed, keeping thus the SNR at maximum;
- A 16-bit DAC to apply an offset;
- A 16-bit ADC to convert the signal.

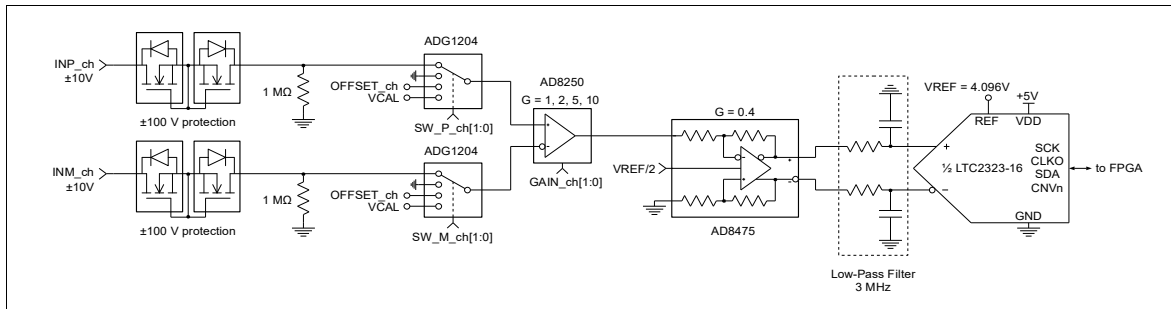


Figure 2 - ADC_3117 ADC Input Stage

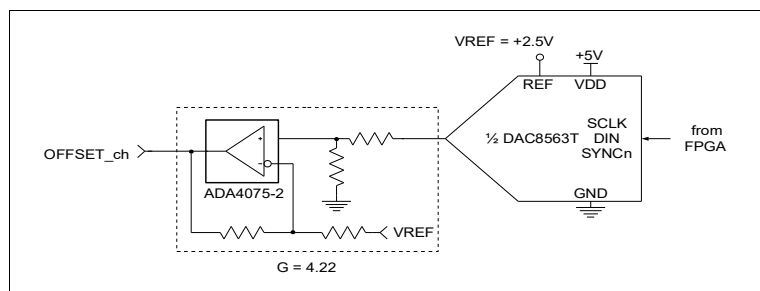


Figure 3 - ADC_3117 ADC Input DC Compensation DAC

The ADC inputs can operate in the following modes:

- **Differential mode:** SW_P_ch and SW_M_ch connects the inputs directly to the instrument amplifier. The input ranges are given in Table 2.2
- **SE bipolar mode:** SW_P_ch in position "direct", SW_M_ch in position GND. Input ranges are the same as in differential mode. It is also possible to set SW_M_ch to GND and use the negative INM_ch input instead. The signal is thus inverted at the ADC input and should be re-inverted by digital processing. In addition, this possibility of using input multiplexing doubles the available number of channels (with limited A/D conversion speed)
- **SE bipolar mode with offset:** same as above, but with SW_M_ch set to "offset". This way, any signal offset between -10 to +10 [V] can be compensated
- **SE unipolar mode:** SW_P_ch set to "direct", SW_M_ch set to "offset" with a fixed value. The available input ranges are given in Table 2.3. This mode also offers the option of using the negative input and digital sign inversion in order to double the number of input channels (with limited A/D conversion speed)

Input range [V]	Exact input range [+/- V]	PGA gain	Diff. Amp gain	ADC diff. Input [+/- V]
-10 to +10	10.24	1	0.4	4.096
-5 to +5	5.12	2	0.4	4.096
-2 to +2	2.05	6	0.4	4.096
-1 to +1	1.02	10	0.4	4.096

Table 2.2 - Differential Input Ranges [-/+]

Input range [V]	Offset DAC [V]	Exact input range [V]	PGA gain	Diff. Amp gain	ADC diff. Input [+/- V]
0 to +10	5.00	10.24	2	0.4	4.096
0 to +4	2.00	4.096	5	0.4	4.096
0 to +2	1.00	2.048	10	0.4	4.096

Table 2.3 - Unipolar Input Ranges

2.2.2.1 ADC Calibration

The front-end can be fully calibrated in terms of both offset and gain with VCAL voltage, unique for the whole mezzanine. The VCAL voltage can be selected from different sources:

- a variable voltage based on a +10V precision voltage reference (REF5010), this voltage is used to calibrate ADC input channel;
- a +4V fixed voltage (based on the +10V precision voltage reference), this voltage is used as reference voltage for the DAC outputs and can be measured with ADC input channel;
- DAC output channel #0 can be measured with ADC input channel;
- DAC output channel #1 can be measured with ADC input channel;

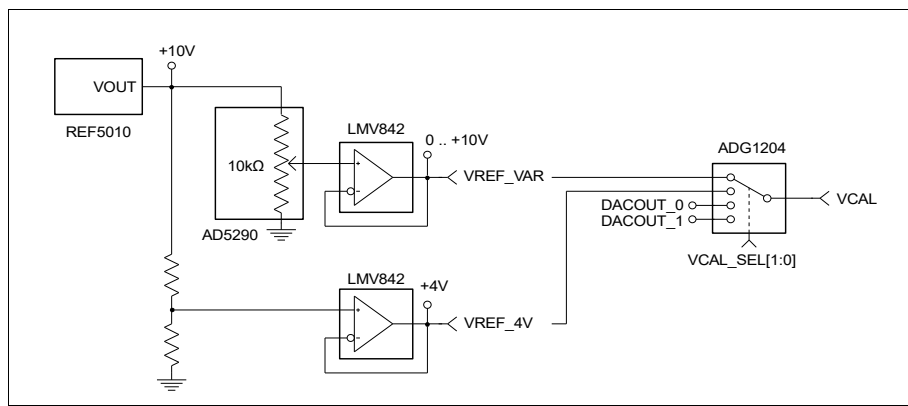


Figure 4 - ADC_3117 VCAL Calibration Sources

The exact +10V precision reference voltage value VCAL is measured at the production stage with a precision voltmeter and stored in EEPROM. The measurement chain offset can be measured by setting both input switches to GND. The gain can be measured with 2 points, by setting one time SW_P_ch to VCAL, SW_M_ch to GND, then the opposite. Then correction values could be applied digitally on each data point with a function of type $y = ax + b$, with a and b stored in EEPROM. Once the channel calibration is done, the offset DAC errors and DAC outputs can also be compensated by comparison and stored.

2.2.2.2 ADC LTC2323-16 Read-Out Interface

The ADC LTC2323-16 read-out is implemented in LVDS mode, for optimal digital implementation.

- High speed LVDS serial interface, up to 110 MHz
- LVDS digital power supply for compatibility with Xilinx Virtex-6T and Kintex UltraScale devices to enable integration in both VME64x and MTCA.4 carriers from IOxOS Technologies
- Mirrored ADC_ch_CLKOUT for high margin set-up/hold time
- Low noise LVDS interface

2.2.2.3 ADC/DAC Low Noise Power Supplies

The ADC_3117 implements specific on-board power supplies for optimal noise reduction. The circuitry infrastructure is based on current (qualified) the ADC_311x implementation.

Note All critical analog related supplies are built with ultra low-noise LDO.

2.2.3 On-board Clock Distribution

The ADC_3117 clock distribution is implemented a low jitter (<100[fs]) clock synthesizer TI LMK04803B.

The input clock reference can be supplied either from the front panel connectors or from the carrier board through the ANSI/VITA57.1 CLK1_C2M signal (LMK_REFCLK_IN). The PLL2 of the synthesizer can also be driven by the on-board low noise local oscillator (Crystak CVHD-037X-100MHz-50ppom).

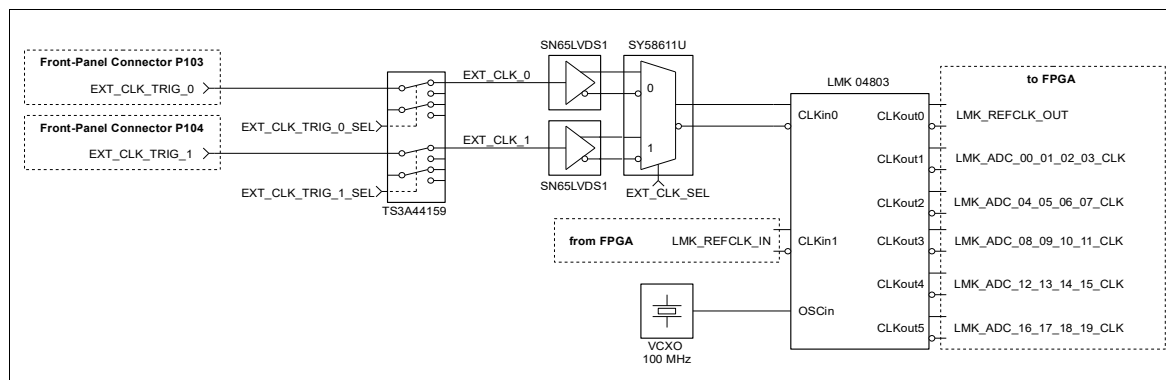


Figure 5 - ADC_3117 Clock Distribution

The Clock source can be selected from:

- FMC ANSI/VITA57.1 LVDS signal generated by carrier FPGA (LMK_REFCLK_IN),
- Front-Panel EXT_CLK_TRIG_0 or EXT_CLK_TRIG_1 reference clock source (shared with GPIOs);
- LMK04803 PLL2 clock, without VCXO;
- LMK04803 PLL2 clock with PLL1 controlled by on-board VCXO, allowing to control the ADC conversion from an external clock reference

The ADC CNVn signal comes directly from FPGA to ADC channel using LVDS pair for optimal signal quality. The clock synthesizer provides 5 dedicated clock to an ADC group and 1 global clock to the FPGA.

2.2.4 DAC Outputs

The ADC_3117 integrates a dual 16-bit DAC (DAC8563T) providing outputs with selectable gain from 0 to ± 10 [V] (using a digital potentiometer).

The DAC outputs are implemented with:

- A dual 16-bit DAC (DAC8563T) with a +4V reference voltage;
- An amplifier to set the output to ± 4 V;
- A digital potentiometer (0 to 10k) and an amplifier to set selectable gain from 0 to 2.5 (digitally programmable);

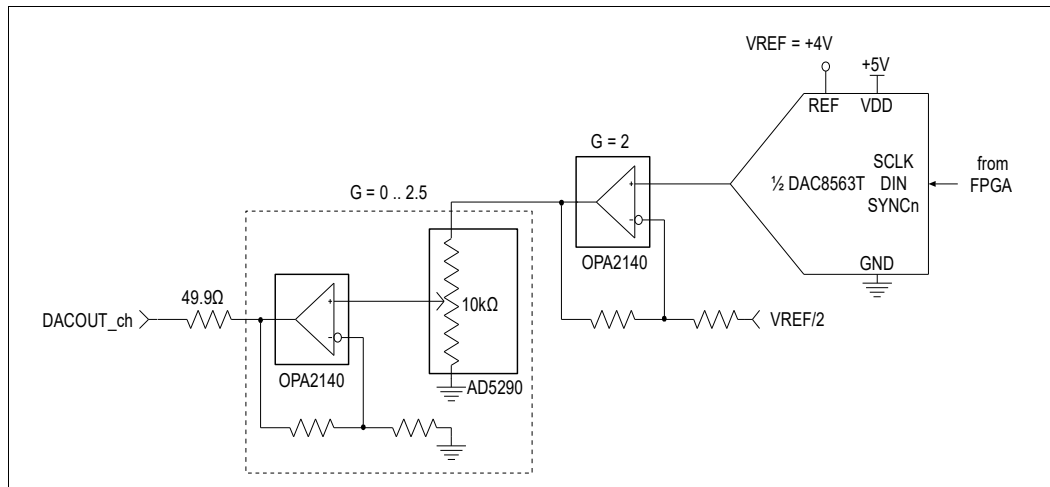


Figure 6 - ADC_3117 DAC Output Chain

The output voltage depends on the programmed DAC value and potentiometer value. The following equations gives the output voltage given D, P:

$$V_{dacout_{ch}}(D, P) = \frac{P}{51} * VREF \left(D - \frac{65535}{2} \right) = \frac{4 * P}{51} \left(D - \frac{65535}{2} \right)$$

Figure 7 - ADC_3117 DAC Output Equation

Where:

D = DAC value (from 0 to 65535)

P = Potentiometer value (from 0 to 255)

VREF = +4V

2.2.5 GPIO Input / Output

The ADC_3117 ADC features two GPIOs in its front panel. These GPIOs are fully programmable from the FMC carrier board and can be used for general purpose application specific as trigger input, trigger output (synchronization purpose) or for event tagging with FPGA specific IP support. The driving section is implemented with standard LVTTTL drivers (± 24 mA) directly controlled by the FMC carrier unit.

The receiving section is implemented with standard LVTTTL buffer. A $33\ \Omega$ resistor is used either as source series termination (when GPIO is used as output) or as $\sim 50\ \Omega$ end termination (when GPIO is used as input).

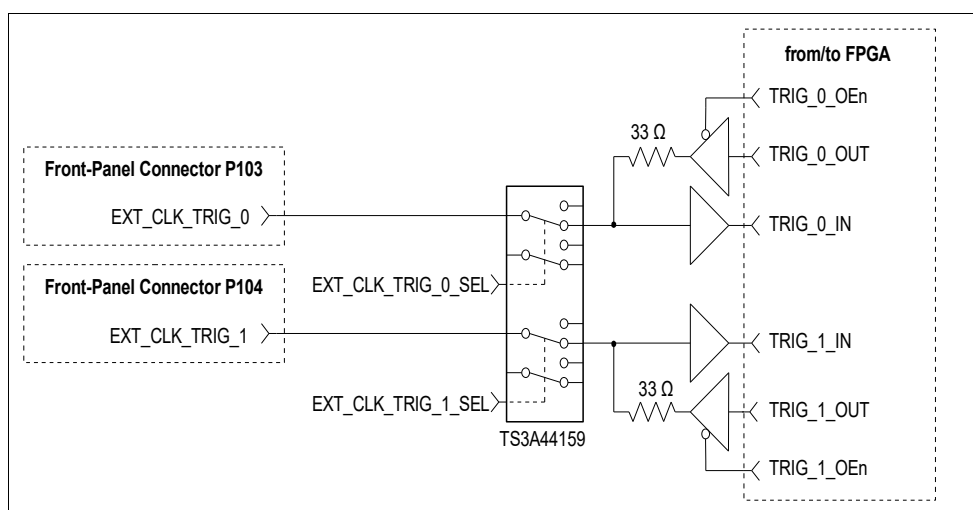


Figure 8 - ADC_3117 GPIO Inputs & Outputs

The functionality is shared with clock inputs from the front-panel.

2.2.6 Serial Interfaces

The ADC_3117 ADC has five(5) dedicated serial interfaces:

- 1x SMBus interface to access to I²C EEPROM (256 [kbit]) and TMP102 thermometer;
- 1 x SPI interface at 26 [MHz] to access eight(8) x XRA1405 used to control ADC gain and switches, VCXO enable, VCAL selection and Clock/Trigger selection;
- 1x uWIRE interface at 20 [MHz] to access LMK04803B (Clock Synthesizer);
- 1x SPI interface at 50 [MHz] to access dual DAC DAC8563T used for analog outputs;
- 1x SPI interface at 50 [MHz] / 4 [MHz] to access ten(10) dual DACs DAC8563T used for ADC offset compensation and three(3) digital potentiometer AD5290 used to control analog outputs and variable calibration voltage;

2.2.7 Visual Indicators

The ADC_3117 provides two(2) LED, directly controlled through the FMC.

A LED controlling block is supplied in VHDL for FPGA integration.

2.2.8 EEPROM Signature

The ADC_3117 has a 256 [kbit] EEPROM (M24256) interfaced through the FMC SMBus (SDA, SDC signals). This non-volatile device can be directly accessed through the FMC Carrier board general I2C Master Controller.

The EEPROM based address is selected with FMC geographic addressing "5xH" as defined by ANSI/VITA 57.1 specification in §5.6.

The ADC_3117 on-board EEPROM is divided in three(3) sections as shown in Table 2.4:

Address range	Comment
0x0000 – 0x1FFF	IPMI parameters as defined in ANSI/VITA 57.1 specification §5.5.
0x2000 – 0x6FFF	ADC_3117 user specific parameter (such as correction values).
0x7000 – 0x7FFF	IOxOS signature (refer to §3.6).

Table 2.4 - ADC_3117 EEPROM Address Mapping

2.2.9 Thermometer TMP102

The ADC_3117 incorporates one on board digital thermometer TMP102 connected on FMC SMBus for on-board temperature monitoring purposes.

2.3 FMC HPC IO Signalling

The ADC_3117 is a ANSI/VITA57.1 single-width FMC Mezzanine Card featuring a High Pin Count (HPC) connector.

2.3.1 FMC General Power

FMC HPC Signalling	Function	ADC_3117 Usage	Comments
3P3V	Power	+3.3[V] Power supply supplied by the Carrier board → 1.2 [A] required	
3P3VAUX	Power	I2C EEPROM and Thermal power → 0.003 [A] required	
VADJ	Power	+1.8 [V] to +2.6 [V] Power supply supplied by the Carrier board → 0.003 [A] required	Use +2.6 [V] for IFC-1210 Use +1.8 [V] for IFC-1211 or IFC-1410
12P0V	Power	+12[V] Power supply → 0.145 [A] required	
PG_M2C	Power	Not used	
PG_C2M	Power	Power Good coming from Carrier board	Control on-board LDO / DCDC, used to reduce inrush current during power-up.
VIO_B	Power	Not used	
VREFA_M2C	I/O Reference	Not used	
VREFB_M2C	I/O Reference	Not used	

Table 2.5 - ADC_3117 FMC Power supplies

2.3.2 FMC General Services

FMC HPC Signalling	Function	ADC_3117 Usage	Comments
CLK0_M2C	Clock	LMK04803 Reference Clock Output	
CLK1_M2C	Clock	LMK04803 Reference Clock Input	
CLK2_BIDIR	Clock	Not used	
CLK3_BIDIR	Clock	Not used	
CLKDIR	Clock	Not used	Pull-up 10K to 3P3V
GBTCLKx_M2C	Clock	Not used	
TRST_L, TMS, TCK	JTAG	Not implemented	JTAG Not supported
TDI, TDO	JTAG	Direct connection between TDI → TDO	
SCL, SDA	I2C	EEPROM 256K interface, TMP102	

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GA[1:0]	GEO_ADDR	FMC geographic addressing	Used to select EEPROM address.
PRST_M2C	PRESENT	Connected to GND	

Table 2.6 - ADC_3117 ANSI/VITA57.1 General signalling

2.3.3 FMC DE LVDS Interface

The ADC_3117 uses LVDS differential signalling for the following functionalities:

- 16-bit ADC LTC2323 read-out,
- LMK04803 dedicated Clock Outputs for a group of four(4) ADCs

FMC HPC Signalling	Function	ADC_3117 Usage	Comments
LA_CC[0]	LMK_ADC_00_01_02_03_CLK	LMK Clock Output	ADC channel #0 - #3
LA[7]	ADC_00_01_SCK	LTC2323 Serial Clock Input	
LA[8]	ADC_02_03_SCK	LTC2323 Serial Clock Input	
LA[6]	ADC_00_01_CNV	LTC2323 Conversion	
LA[11]	ADC_02_03_CNV	LTC2323 Conversion	
LA_CC[1]	ADC_00_01_CLKOUT	LTC2323 Clock Output	
LA[19]	ADC_02_03_CLKOUT	LTC2323 Clock Output	
LA[2]	ADC_00_SDO	LTC2323 Serial Data Output	
LA[3]	ADC_01_SDO	LTC2323 Serial Data Output	
LA[4]	ADC_02_SDO	LTC2323 Serial Data Output	
LA[5]	ADC_03_SDO	LTC2323 Serial Data Output	
LA_CC[17]	LMK_ADC_04_05_06_07_CLK	LMK Clock Output	ADC channel #4 - #7
LA[9]	ADC_04_05_SCK	LTC2323 Serial Clock Input	
LA[10]	ADC_06_07_SCK	LTC2323 Serial Clock Input	
LA[12]	ADC_04_05_CNV	LTC2323 Conversion	
LA_CC[18]	ADC_06_07_CNV	LTC2323 Conversion	
LA[20]	ADC_04_05_CLKOUT	LTC2323 Clock Output	
LA[21]	ADC_06_07_CLKOUT	LTC2323 Clock Output	
LA[13]	ADC_04_SDO	LTC2323 Serial Data Output	
LA[14]	ADC_05_SDO	LTC2323 Serial Data Output	
LA[15]	ADC_06_SDO	LTC2323 Serial Data Output	
LA[16]	ADC_07_SDO	LTC2323 Serial Data Output	
HA_CC[0]	LMK_ADC_08_09_10_11_CLK	LMK Clock Output	ADC channel #8 - #11
HA[6]	ADC_08_09_SCK	LTC2323 Serial Clock Input	

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HA[7]	ADC_10_11_SCK	LTC2323 Serial Clock Input	
HA[4]	ADC_08_09_CNV	LTC2323 Conversion	
HA[5]	ADC_10_11_CNV	LTC2323 Conversion	
HA[1]	ADC_08_09_CLKOUT	LTC2323 Clock Output	
LA[33]	ADC_10_11_CLKOUT	LTC2323 Clock Output	
HA[2]	ADC_08_SDO	LTC2323 Serial Data Output	
HA[3]	ADC_09_SDO	LTC2323 Serial Data Output	
HA[8]	ADC_10_SDO	LTC2323 Serial Data Output	
HA[9]	ADC_11_SDO	LTC2323 Serial Data Output	
HA_CC[17]	LMK_ADC_12_13_14_15_CLK	LMK Clock Output	ADC channel #12 - #15
HA[10]	ADC_12_13_SCK	LTC2323 Serial Clock Input	
HA[16]	ADC_14_15_SCK	LTC2323 Serial Clock Input	
HA[13]	ADC_12_13_CNV	LTC2323 Conversion	
HA[19]	ADC_14_15_CNV	LTC2323 Conversion	
HB[11]	ADC_12_13_CLKOUT	LTC2323 Clock Output	
HA_CC[18]	ADC_14_15_CLKOUT	LTC2323 Clock Output	
HA[11]	ADC_12_SDO	LTC2323 Serial Data Output	
HA[12]	ADC_13_SDO	LTC2323 Serial Data Output	
HA[14]	ADC_14_SDO	LTC2323 Serial Data Output	
HA[15]	ADC_15_SDO	LTC2323 Serial Data Output	
HB_CC[0]	LMK_ADC_16_17_18_19_CLK	LMK Clock Output	ADC channel #16 - #19
HB[2]	ADC_16_17_SCK	LTC2323 Serial Clock Input	
HB[9]	ADC_18_19_SCK	LTC2323 Serial Clock Input	
HB[1]	ADC_16_17_CNV	LTC2323 Conversion	
HB[5]	ADC_18_19_CNV	LTC2323 Conversion	
HB_CC[6]	ADC_16_17_CLKOUT	LTC2323 Clock Output	
HB[10]	ADC_18_19_CLKOUT	LTC2323 Clock Output	
HB[3]	ADC_16_SDO	LTC2323 Serial Data Output	
HB[4]	ADC_17_SDO	LTC2323 Serial Data Output	
HB[7]	ADC_18_SDO	LTC2323 Serial Data Output	
HB[8]	ADC_19_SDO	LTC2323 Serial Data Output	

Table 2.7 - ADC_3117 FPGA LVDS IO Signalling

2.3.4 FMC SE Interface

The ADC_3117 uses the LVCMOS for the following functionalities:

- LMK04803 uWIRE interface and status signals;
- ADC Offset Compensation DAC SPI interface;
- Trigger Input / Output interface;
- XRA1405 SPI interface;
- Dedicated DAC Outputs SPI interface;
- Programmable Visual Indicators;
- VCXO Enable;
- Thermal Alert;

FMC HPC Signalling	Function	Signal Name	ADC_3117 Usage	Comments
LA[23P]	Control	LMK_LE	LMK uWIRE LE	LMK04803 Interface
LA[23N]	Control	LMK_SDAT	LMK uWIRE DATA	
LA[24P]	Control	LMK_SCLK	LMK uWIRE SCLK	
LA[30N]	Status	LMK_STA_CLKIN0	LMK Status Clock Input #0	
LA[24N]	Status	LMK_STA_CLKIN1	LMK Status Clock Input #1	
LA[25P]	Status	LMK_STA_LD	LMK Lock Detect	
LA[25N]	Status	LMK_STA_HOLD OVER	LMK Readback Output	
LA[26P]	Status	LMK_SYNCn	LMK Synchronization Input	
LA[26N]	Control	ADC_DAC_CLRn	DACs Clear Input	ADC Offset Compensation DAC Interface
LA[27P]	Control	ADC_DAC_DIN	SPI Data Input	
LA[27N]	Control	ADC_DAC_SCLK	SPI Clock	
LA[28P]	Control	ADC_DAC_SYNCn	SPI Chip Select	
LA[28N]	Control	ADC_DAC_SEL[0]	SPI Device Select Bit #0	
LA[29P]	Control	ADC_DAC_SEL[1]	SPI Device Select Bit #1	
LA[29N]	Control	ADC_DAC_SEL[2]	SPI Device Select Bit #2	
LA[30P]	Control	ADC_DAC_SEL[3]	SPI Device Select Bit #3	
LA[31N]	Status	TRIG_0_IN	Trigger #0 Input	Trigger Inputs / Outputs
LA[32P]	Control	TRIG_0_OUT	Trigger #0 Output	
LA[32N]	Control	TRIG_0_OEn	Trigger #0 Output Enable	
HB[18N]	Status	TRIG_1_IN	Trigger #1 Input	
HB[18P]	Control	TRIG_1_OUT	Trigger #1 Output	
HB[19P]	Control	TRIG_1_OEn	Trigger #0 Output Enable	

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HB[12P]	Control	XRA1405_CS[n][0]	XRA1405 Chip Select #0	XRA1405 GPIO Extender Interface
HB[12N]	Control	XRA1405_CS[n][1]	XRA1405 Chip Select #1	
HB[13P]	Control	XRA1405_CS[n][2]	XRA1405 Chip Select #2	
HB[13N]	Control	XRA1405_CS[n][3]	XRA1405 Chip Select #3	
HB[14P]	Control	XRA1405_CS[n][4]	XRA1405 Chip Select #4	
HB[14N]	Control	XRA1405_CS[n][5]	XRA1405 Chip Select #5	
HB[15P]	Control	XRA1405_CS[n][6]	XRA1405 Chip Select #6	
HB[15N]	Control	XRA1405_CS[n][7]	XRA1405 Chip Select #7	
HB[16P]	Control	XRA1405_SCL	XRA1405 Serial Clock	
HB[16N]	Control	XRA1405_SI	XRA1405 Serial Data Input	
HA[20P]	Control	DAC_0_1_CLRn	DAC Clear Input	DAC Outputs Interface
HA[20N]	Control	DAC_0_1_DIN	SPI Data Input	
HA[21P]	Control	DAC_0_1_SCLK	SPI Clock	
HA[21N]	Control	DAC_0_1_SYNCn	SPI Chip Select	
LA[22P]	Control	LED_G0n	Green LED	Programmable Visual Indicators
LA[22N]	Control	LED_R0n	Red LED	
LA[31P]	Control	VCXO_100M_EN	Enable VCXO	VCXO Interface
HB[20P]	Status	TMP102_ALERTn	Thermal Alert	TMP102 Interface

Table 2.8 - ADC_3117 FPGA SE LVMOS IO Signalling

2.4 Mechanical Informations

The ADC_3117 complies with ANSI/VITA57.1 Single-Width FMC Mezzanine Card with stacking height of 8.5 [mm] and 10 [mm].

2.4.1 Front Panel

The ADC_3117 front panel has two (2) SDR Connectors from 3M P103 and P104.

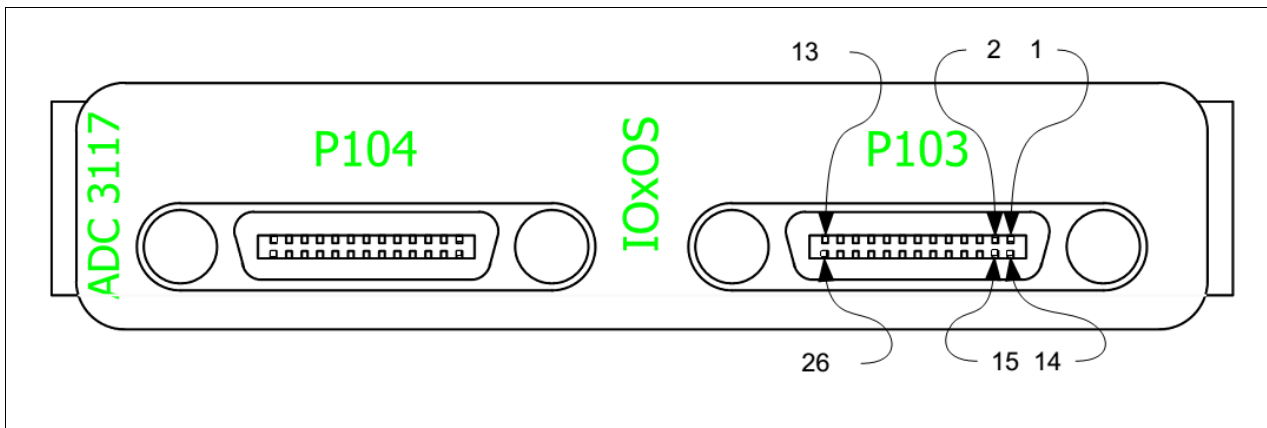


Figure 9 - ADC_3117 Front Panel Mechanical Drawing

2.4.2 P103 Connector Pinout

Name	Pin Number		Name	Comments
EXT_CLK_TRIG_0	1	14	GND	
DACOUT_0	2	15	GND	Twisted Pair
INM_00	3	16	INP_00	Twisted Pair
INM_01	4	17	INP_01	Twisted Pair
INM_02	5	18	INP_02	Twisted Pair
INM_03	6	19	INP_03	Twisted Pair
INM_04	7	20	INP_04	Twisted Pair
INM_05	8	21	INP_05	Twisted Pair
INM_06	9	22	INP_06	Twisted Pair
INM_07	10	23	INP_07	Twisted Pair
INM_08	11	24	INP_08	Twisted Pair
INM_09	12	25	INP_09	Twisted Pair
GND	13	26	GND	

Table 2.9 - ADC_3117 P103 Connector Pinout

2.4.3 P104 Connector Pinout

Name	Pin Number		Name	Comments
EXT_CLK_TRIG_1	1	14	GND	
DACOUT_1	2	15	GND	Twisted Pair
INM_10	3	16	INP_10	Twisted Pair
INM_11	4	17	INP_11	Twisted Pair
INM_12	5	18	INP_12	Twisted Pair
INM_13	6	19	INP_13	Twisted Pair
INM_14	7	20	INP_14	Twisted Pair
INM_15	8	21	INP_15	Twisted Pair
INM_16	9	22	INP_16	Twisted Pair
INM_17	10	23	INP_17	Twisted Pair
INM_18	11	24	INP_18	Twisted Pair
INM_19	12	25	INP_19	Twisted Pair
GND	13	26	GND	

Table 2.10 - ADC_3117 P104 Connector Pinout

2.4.4 P104 Connector Pinout

The 3M SDR cable 1SD26-3120-00C-XXX (XXX = 200 / 500 / A00) must be used to connect equipment to ADC-3117.

ADC-3117 Connector Pin Number	ADC-3117 P103 Connector Signal Name	ADC-3117 P104 Connector Signal Name	Equipment Connector Pin Number	Comments
2	DACOUT_0	DACOUT_1	25	
15	GND	GND	12	
3	INM_00	INM_10	24	
16	INP_00	INP_10	11	
4	INM_01	INM_11	23	
17	INP_01	INP_11	10	
5	INM_02	INM_12	22	
18	INP_02	INP_12	9	
6	INM_03	INM_13	21	
19	INP_03	INP_13	8	

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7	INM_04	INM_14	20	
20	INP_04	INP_14	7	
8	INM_05	INM_15	19	
21	INP_05	INP_15	6	
9	INM_06	INM_16	18	
22	INP_06	INP_16	5	
10	INM_07	INM_17	17	
23	INP_07	INP_17	4	
11	INM_08	INM_18	16	
24	INP_08	INP_18	3	
12	INM_09	INM_19	15	
25	INP_09	INP_19	2	
1	EXT_CLK_TRIG_0	EXT_CLK_TRIG_1	1	
26	GND	GND	26	
13	GND	GND	13	
14	GND	GND	14	

Table 2.11 - SDR Cable Pinout

2.4.5 PCB Layout Implementation

The ADC_3117 is implemented with a 12-layer PCB organized in three main sections:

- Front-end section → ADC analog pre-amplifier
- Middle section → ADC converter, analog/digital
- Back-end section → Power supplies (LDO and DC/DC) and GPIO. This section is optimized for thermal evacuation and minimal noise and induced current perturbation.

The ADC_3117 features two(2) 3M SDR Connectors (Part Number 12226-8250-00FR) in its front panel with the mechanical drawing showed in Figure 10.

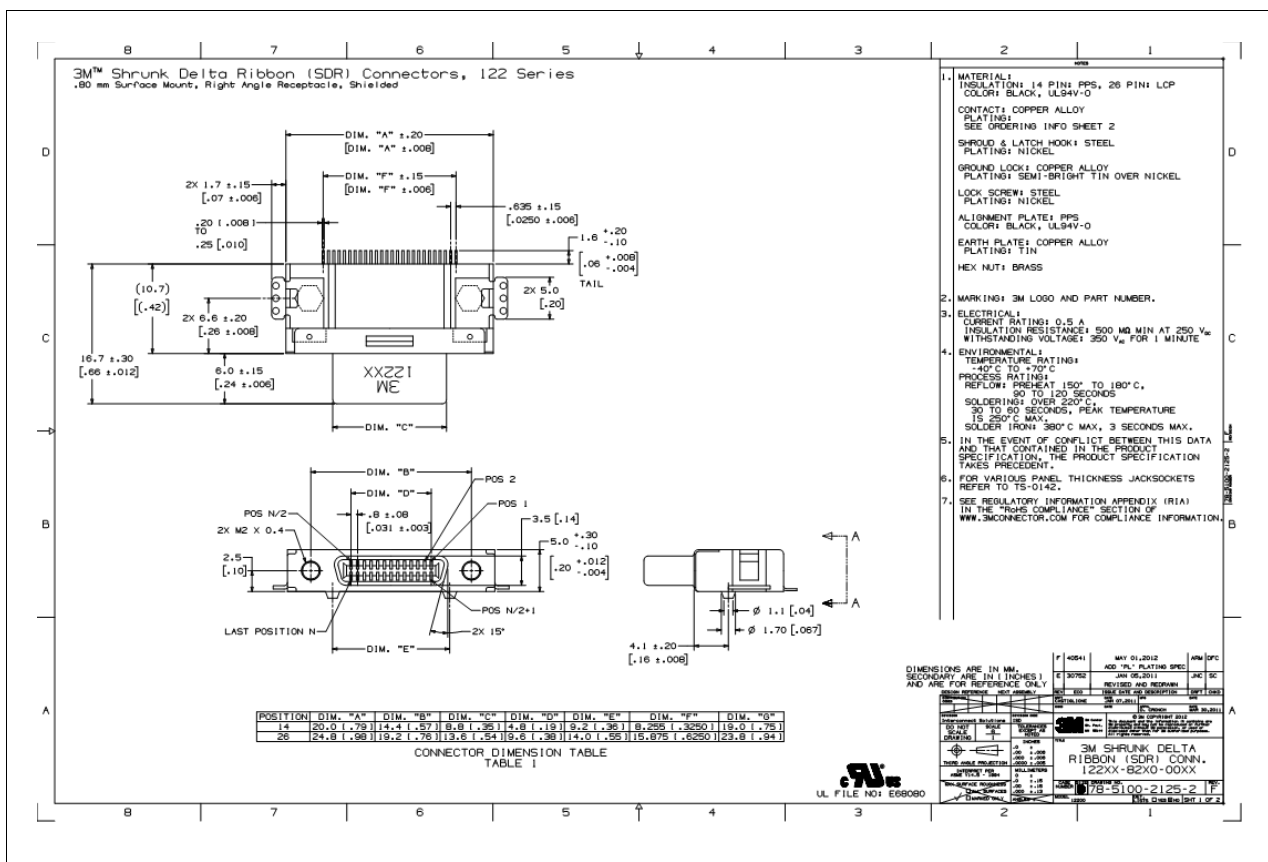


Figure 10 - 3M SDR Connector Mechanical Drawing

3. FPGA Firmware Support

This section describes the functions integrated in the FMC carrier FPGA to enable the implementation of data-acquisition applications using the ADC_3117 High-Density ADC FMC board.

3.1 ADC_3117 VHDL Specific

3.1.1 ADC/DAC Device Support

Section to be completed in next release of this Technical Specification.

3.1.2 TCSR Resources

Section to be completed in next release of this Technical Specification.

3.2 XUSER Support

Section to be completed in next release of this Technical Specification.